Amendments to the Claims

Claims 1-6 (Canceled)

7. (Currently Amended) An interface apparatus comprising:

a processor for receiving at least one network interface signal, and for recognizing a transport mechanism associated with each network interface signal;

a bus interface device for generating at least one system interface signal in response to the recognized transport mechanism; wherein:

the transport mechanism comprises at least one of Asynchronous Transfer Mode, Internet Protocol, Frame Relay, Integrated Services Digital Network, High bit-rate Digital Subscriber Line, Asymmetric Digital Subscriber Line, Very High Data Rate Digital Subscriber Line, Symmetric Digital Subscriber Line, 10 base T, 100 base T, Gigabit Ethernet and E1/T1;

the processor further examines a pattern for each network interface signal to recognize the associated transport mechanism;

each system interface signal is coupled with at least one of a circuit switched interface, a packet switched interface, and a combined circuit packet switched interface;

the transport mechanism comprises an adaptation layer of Asynchronous Transfer Mode, the processor performs ATM adaptation layer processing on each Network Interface signal in response to the recognized transport mechanism; and

~~The interface apparatus of Claim 6, wherein~~ at least one of the processor and the bus interface device matches a timing of the circuit switched interface and formats the ATM adaptation layer processed ~~Network Interface~~ network interface signal to the corresponding ~~System Interface~~ system interface signal.

8. (Currently Amended) The interface apparatus of Claim 7, comprising a control switch for partitioning and switching the performance of the matching the

timing and the performance of the formatting the ATM adaptation layer processed ~~Network Interface~~ network interface signal between the processor and the bus interface device in response to a control signal.

9. (Canceled)

10. (Currently Amended) An interface apparatus comprising:

a processor for receiving at least one network interface signal, and for recognizing a transport mechanism associated with each network interface signal;

a bus interface device for generating at least one system interface signal in response to the recognized transport mechanism; wherein:

the transport mechanism comprises at least one of Asynchronous Transfer Mode, Internet Protocol, Frame Relay, Integrated Services Digital Network, High bit-rate Digital Subscriber Line, Asymmetric Digital Subscriber Line, Very High Data Rate Digital Subscriber Line, Symmetric Digital Subscriber Line, 10 base T, 100 base T, Gigabit Ethernet and E1/T1;

the processor further examines a pattern for each Network Interface signal to recognize the associated transport mechanism;

each system interface signal is coupled with at least one of a circuit switched interface, a packet switched interface, and a combined circuit packet switched interface;

at least one of the processor and the bus interface device converts each network interface signal to correspond with the packet switched interface and routes each converted network interface signal; and

~~The~~ the interface apparatus ~~of Claim 9, comprising~~ further comprises a control switch for partitioning and switching the performance of ~~the converting each Network Interface signal and the routing each converted Network Interface signal~~ each said network interface signal conversion and each said network

interface signal routing in response to a control signal between the processor and the bus interface device.

Claims 11-20 (Canceled)